(19) (11) Publication number: 10012886 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 08164090

(51) Intl. Cl.: H01L 29/786 H01L 21/336

(22) Application date: 25.06.96

(30) Priority:

(43) Date of application publication: 16.01.98

(84) Designated contracting states:

(71) Applicant: HITACHI LTD

(72) Inventor: HATANO MUTSUKO
AKIMOTO HAJIME

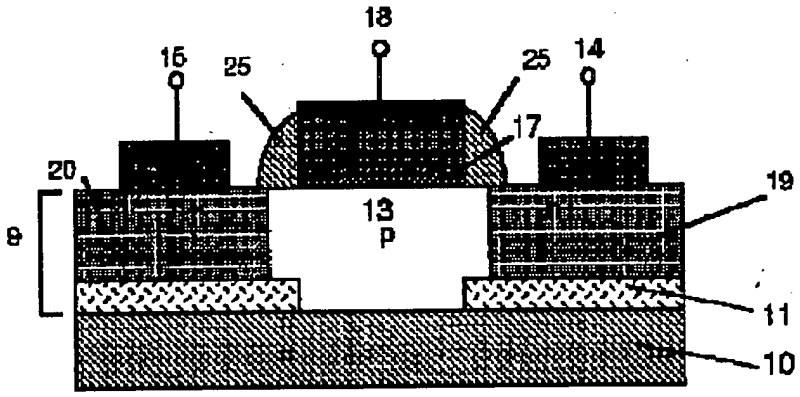
(74) Representative:

(54) SEMICONDUCTOR DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To suppress the substrate floating effect of a semiconductor device having a MIS field effect transistor on a semiconductor layer by forming at least one region having a recombination center structure for ionized charges in a polycrystalline Si film.

SOLUTION: An n-type MIS transistor comprises an insulative substrate 10, polycrystalline Si layer 9 deposited on the substrate, source diffused layer 20, source electrode 15 connected thereto, drain diffused layer 19, drain electrode 14 connected thereto, and gate electrode 18 connected through a gate insulation film 17 in the Si layer 9. Crystal defects are locally caused in a part between the transistor and substrate 10 at desired positions and depth by implanting ions of an element e.g. Si, Ar and Ne in the Si layer 9 to form regions 11 as recombination centers. Thus it is possible to suppress the substrate floating effect with holding the high speed and low operating voltage features owing to a low parasitic capacitance of the thin film transistor to obtain a high reliability semiconductor device.



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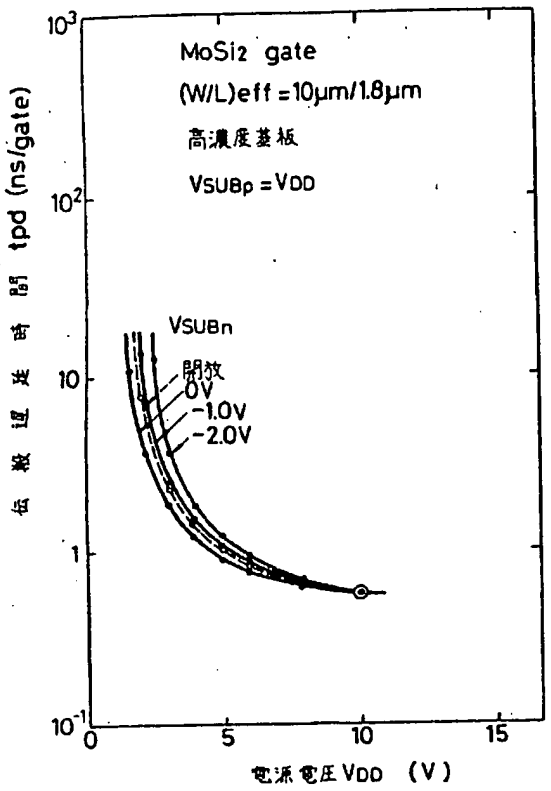
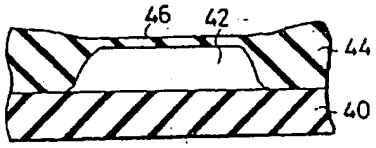
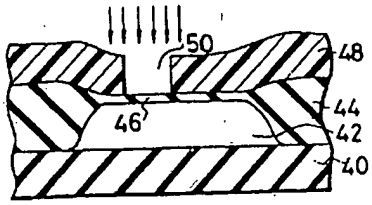


第 5a 図



第 5b 図



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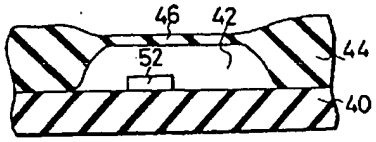
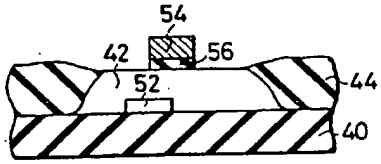
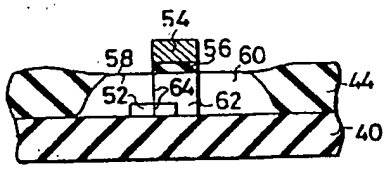


第 5d 図



第 5e 図



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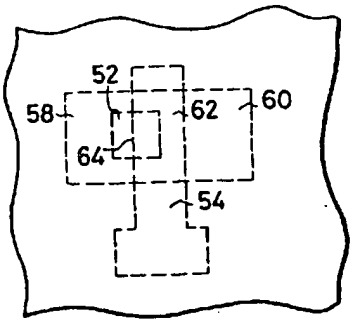
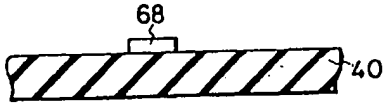
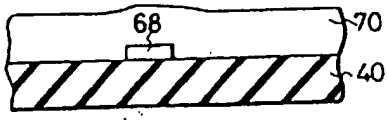


第 7a 図

第 7b 図



第 7c 図



(19) (11) Publication number: 58015274 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 56113236

(51) Intl. Cl.: H01L 29/78 H01L 27/12

(22) Application date: 20.07.81

(30) Priority:

(43) Date of application publication: 28.01.83

(84) Designated contracting states:

(71) Applicant: TOSHIBA CORP

(72) Inventor: TAGUCHI SHINJI

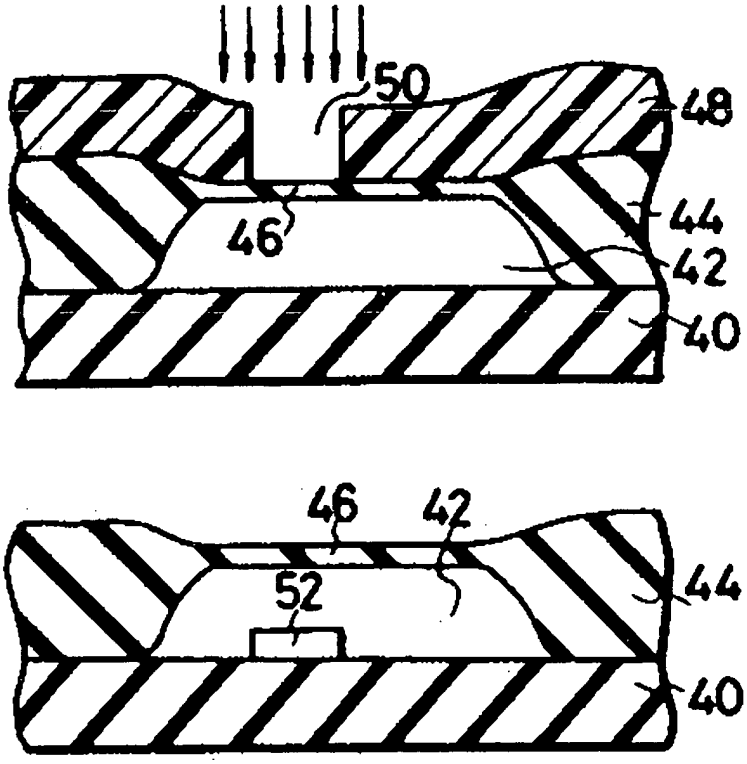
(74) Representative:

(54) MOS SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57) Abstract:

PURPOSE: To obtain an MOS semiconductor which does not generate substrate floating effect without decreasing the integration by disordering at least a part of crystallinity of a p-n junction except the surface of a semiconductor region of the p-n junction formed between a substrate region and an impurity region.

CONSTITUTION: A single crystal silicon region 42 and a field oxidized film 44 are fored on an insulating substrate 40, and an SiO2 layer 46 is further formed. After a resist 48 is then accumulated, it is selectively etched to form a hole 50 reaching the layer 46. Thereafter, Si ions are injected under the conditions of accelerating voltage of 190keV and dosage of 1 × 1016/cm2. Under these conditions, projected resin RP is 2,952Å and is disposed at the boundary between a silicon and a sapphire. Accordingly, a crystalline deterioration region 52 is formed in the boundary between a single crystal silicon region 42 and an insulating substrate 40 of the sapphire. In the region 52, the lattice defects exist more conspicuously in the single crystal silicon region 42 around the periphery, and the crystal orientation is disordered.



(19) (11) Publication number: **03032064 A**

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: 01167597

(51) Intl. Cl.: H01L 29/784

(22) Application date: 29.06.89

(30) Priority:

(43) Date of application publication: 12.02.91

(84) Designated contracting states:

(71) Applicant: MITSUBISHI ELECTRIC CORP

(72) Inventor: ODA SHUICHI

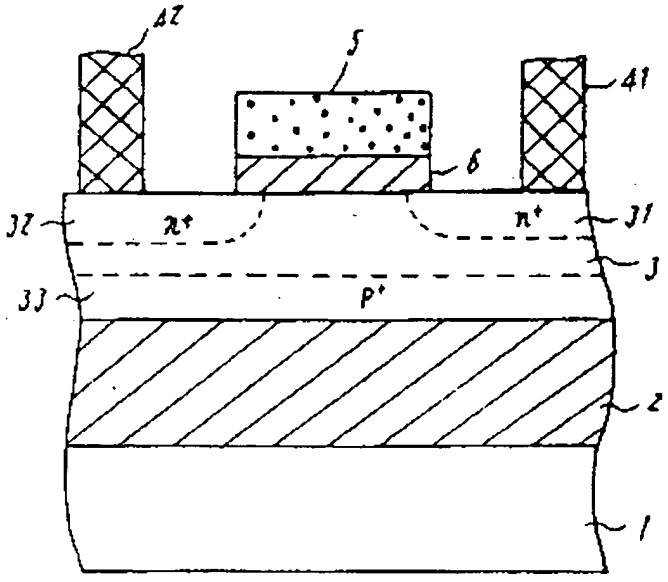
(74) Representative:

(54) SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: In a transistor being formed within the silicon film on an insulating film, to absorb positive holes generated by collision ionization phenomena so as to improve breakdown strength by providing a region having a concentration higher than the substrate concentration.

CONSTITUTION: When a source electrode 42 is grounded and positive voltage is applied to a gate electrode 5, a transistor becomes ON conditions. When positive voltage is applied to a drain electrode 41 in this condition, electrons flow from a source diffusion layer 32 to a drain diffusion layer 31. Moreover, when the electrons get energy enough being accelerated by an electric field, they collide against a silicon lattice and generate electron-hole pairs, and the electrons generated here are absorbed in a layer 31 along a drain electric field. the positive holes flow in a substrate and are absorbed in a P+ diffusion layer 33 in high positive hole density. Hereby, they do not accumulate in the vicinity of the layer 32, and also potential barriers between the source and the substrate cease to be low. As a result, kink phenomena become small or cease to appear.



(19) (11) Publication number: 09139434 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 07296472

(51) Intl. Cl.: H01L 21/8238 H01L 27/092 H01L 29/786

(22) Application date: 15.11.95

(30) Priority:

(43) Date of application publication: 27.05.97

(84) Designated contracting states:

(71) Applicant: HITACHI LTD

(72) Inventor: HORIUCHI KATSUTADA
IKEDA TAKAHIDE
HIGUCHI HISAYUKI

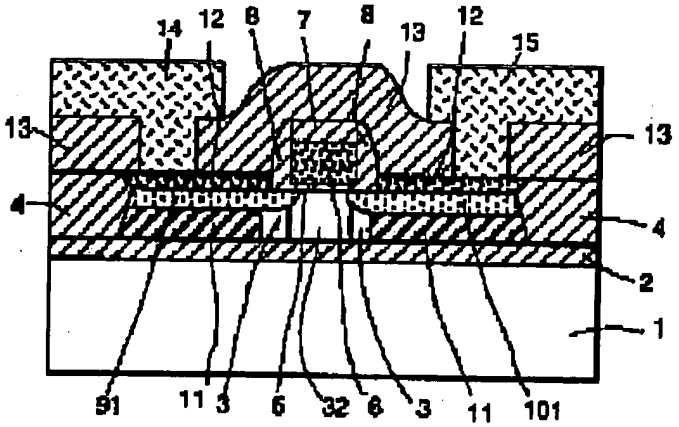
(74) Representative:

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57) Abstract:

PROBLEM TO BE SOLVED: To make it possible to remove the substrate floating effect of a MOS transistor by a method wherein a low density diffusion layer region is provided in the vicinity of the source diffusion layer region of the MOS transistor, and a region having a recombination center structure is provided in the low density diffusion layer region.

SOLUTION: A MOS type field effect transistor, which is formed on a SOI substrate 1, is provided. The high density n-type source diffusion layer 91 of the above-mentioned MOS transistor has the first diffusion layer 12 which is connected to a source electrode 14, and the second diffusion layer of a low impurity density region 3 which is at least in the neighborhood of the lower region of the first diffusion layer 12. Also, a region (crystal defective region) 11, having a recombination center mechanism relative to electric charge, is provided inside the second diffusion layer 3. As a result, the minority carrier generated on the SOI substrate 1 can be implanted into the crystal defective region 11 and annihilated, and the substrate floating effect is cancelled.



3: n⁻
91/101 : S/D : n+.
11 : doped with Ar, or Ne, or Si, Ge, C

(19)

(11) Publication number: **01307268 A**

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 63138884

(51) Intl. Cl.: H01L 29/78 H01L 21/20 H01L 27/12

(22) Application date: 06.06.88

(30) Priority:

(43) Date of application publication: 12.12.89

(84) Designated contracting states:

(71) Applicant: NIPPON TELEGR & TELEPH CORP <NTT>

(72) Inventor: AOKI TAKAHIRO
TOMIZAWA MASAAKI
YOSHII AKIRA

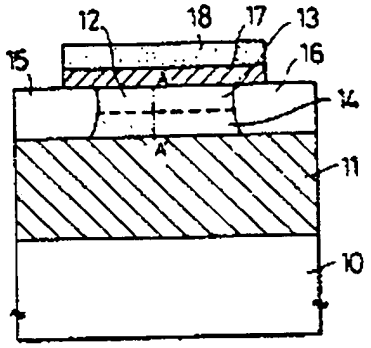
(74) Representative:

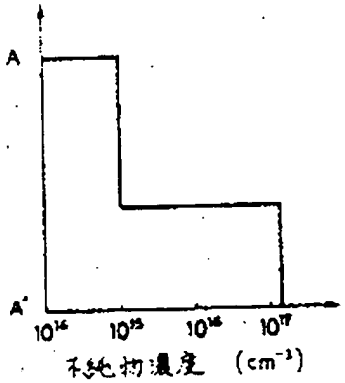
(54) MIS TYPE TRANSISTOR

(57) Abstract:

PURPOSE: To obtain a normally-off MISFET having no kink characteristic and high Gm (mobility) by bringing the surface to low concentration and the base to high concentration in the impurity concentration distribution of a thin-film SOI substrate.

CONSTITUTION: Source-drain regions 15, 16 are formed to the surface of a single crystal silicon layer (an SOI substrate) 12, and an N+ polysilicon gate electrode 18 is shaped onto a channel region between these source-drain regions 15, 16 through a gate insulating film 17. Impurity concentration distribution just under a channel is set so that threshold voltage is brought to the state of normally-off and kind characteristics are not acquired. The thickness of an insulator film 11 is brought to a value not affected by an SOI channel, and the thickness of 30nm of the surface of the SOI substrate 12 is brought to a P type and impurity concentration of 1015cm-3 and the thickness of 20nm of the base of the SOI substrate 12 to the P type and impurity concentration of 2 × 1017cm-3, thus controlling threshold voltage to a normally-off type. Accordingly, the normally-off of high Gm can be realized.





(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **07015015 A**

(43) Date of publication of application: **17 . 01 . 95**

(51) Int. Cl **H01L 29/786**
H01L 21/336

(21) Application number: **06078654**

(22) Date of filing: **18 . 04 . 94**

(30) Priority: **30 . 04 . 93 US 93 56042**

(71) Applicant: **INTERNATL BUSINESS MACH CORP <IBM>**

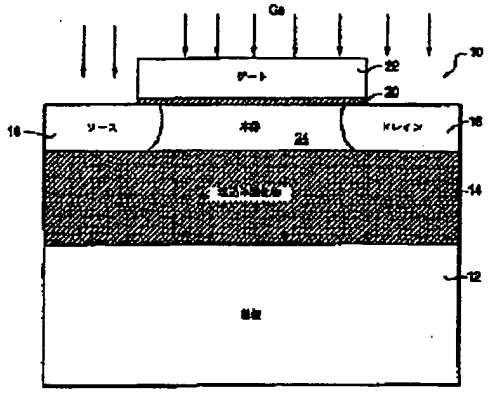
(72) Inventor: **BRADY FREDERICK T**
HADDAD NADIM F
EDENFELD ARTHUR

(54) **METHOD FOR FORMING INTEGRATED CIRCUIT**

(57) Abstract:

PURPOSE: To prevent a latch-up and to increase the breakdown voltage by implanting neutral impurity ions into a silicon transistor element.

CONSTITUTION: An element 10 has a substrate 12, a buried insulating oxide 14, a drain region 16 and a source region 18. A main body region 24 is a channel region under a gate between the source region and the drain region of the element. In a treatment operation, an annealing treatment is performed after neutral species are implanted to remove a damage caused by implantation. Since the neutral impurities include VIII group atoms such as krypton, xenon, germanium and the atoms are large in size and cause turbulence in a band structure, the scattering centers to high energy carriers in a transistor increases. When a drain field having a neutral impurity center is constant, a collision ionization current decreases and a parasitic bipolar effect also decreases, which can prevent a latch-up and increase the breakdown voltage.



(19) (11) Publication number: 61032470 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 59152472

(51) Intl. Cl.: H01L 29/78 H01L 27/12

(22) Application date: 23.07.84

(30) Priority:

(43) Date of application publication: 15.02.86

(84) Designated contracting states:

(71) Applicant: TOSHIBA CORP

(72) Inventor: NOGUCHI TATSUO

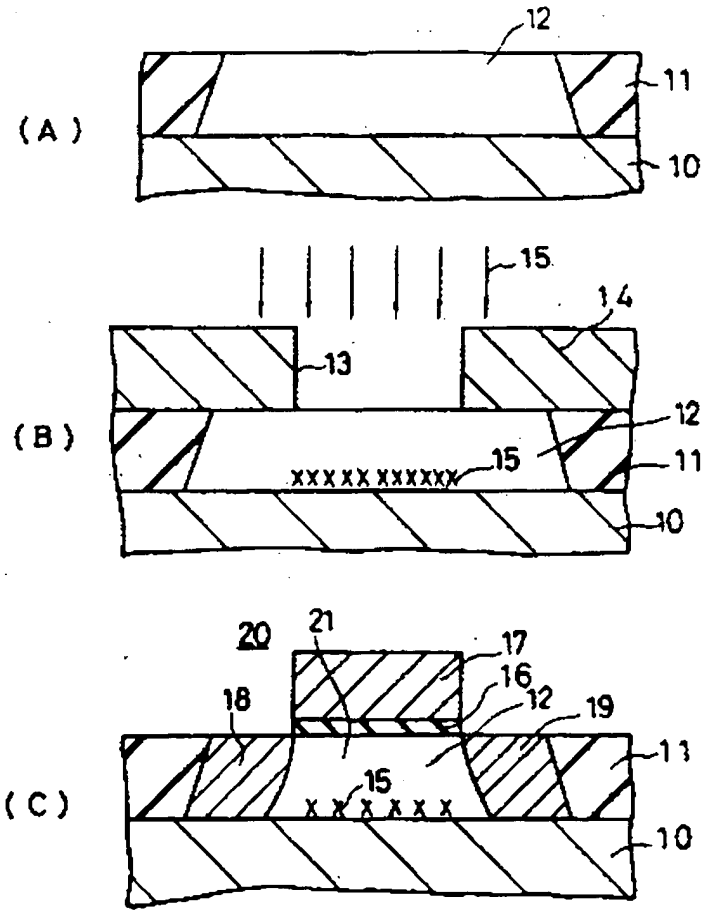
(74) Representative:

(54) MANUFACTURE OF MOS TYPE , SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: To easily obtain the titled device by the simple manufacturing process which is markedly reduced in leakage current generated under the electric floatation of a substrate, by providing the process of introducing an impurity serving as the lifetime killer deeply into the channel which has been formed in the substrate.

CONSTITUTION: A resist film 14 having an aperture 13 by corresponding to the channel forming region in an element region 12 is formed on a field insulation film 11 including the element region 12. Next, the condition for ion implantation is so set that the doping center comes below the channel forming region at a depth distant from the main surface of the element region 12, and the lifetime killer 15 made of an impurity such as Au is injected by using this resist film 14 as a mask. Next, a gate insulation film 16 and a gate electrode 17 are formed on the element region 12 after removal of the resist film 14, which are then patterned. A souce region 18 and a drain region 19 are formed by introducing a required impurity into the element region 12, using that pattern as a mask; accordingly, a semiconductor device 20 is obtained.



(19) (11) Publication number: 04116984 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 02237347

(51) Intl. Cl.: H01L 29/784

(22) Application date: 07.09.90

(30) Priority:

(43) Date of application publication: 17.04.92

(84) Designated contracting states:

(71) Applicant: SEIKO EPSON CORP

(72) Inventor: IWAMATSU SEIICHI

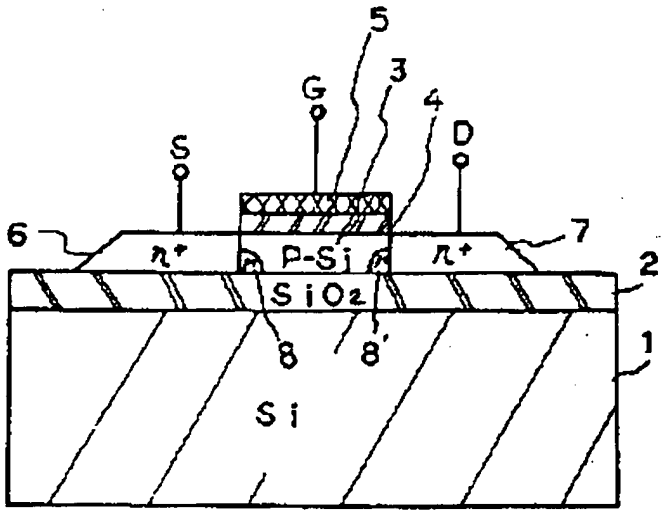
(74) Representative:

(54) N-CHANNEL MOS THIN FILM SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: To perform an N-channel MOS type thin film transistor having high OFF withstand voltage by providing a P+ type diffused layer under a gate adjacent to an N+ type source diffused layer in an N-channel MOS type thin film semiconductor device.

CONSTITUTION: A P-type thin Si film 3, is formed on an SiO2 film 2 formed on an Si substrate 1, and a gate electrode 5, and an N+ type source diffused layer 6, an N+ type drain diffused layer 7 are formed. Further, P+ type diffused layers 8, 8' are formed by an oblique ion implanting method, etc., in such a manner that the layer 8 is adjacent to the layer 6. Thus, the layer 8 is formed so that holes are sunk, thereby improving its OFF withstand voltage.



(19) (11) Publication number: 05198804 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 04180871

(51) Intl. Cl.: H01L 29/784

(22) Application date: 08.07.92

(30) Priority: 25.07.91 JP 03186128

(43) Date of application publication: 06.08.93

(84) Designated contracting states:

(71) Applicant: MATSUSHITA ELECTRIC IND CO LTD

(72) Inventor: HORI ATSUSHI
SEGAWA MIZUKI
SHIMOMURA HIROSHI
KAMEYAMA SHUICHI

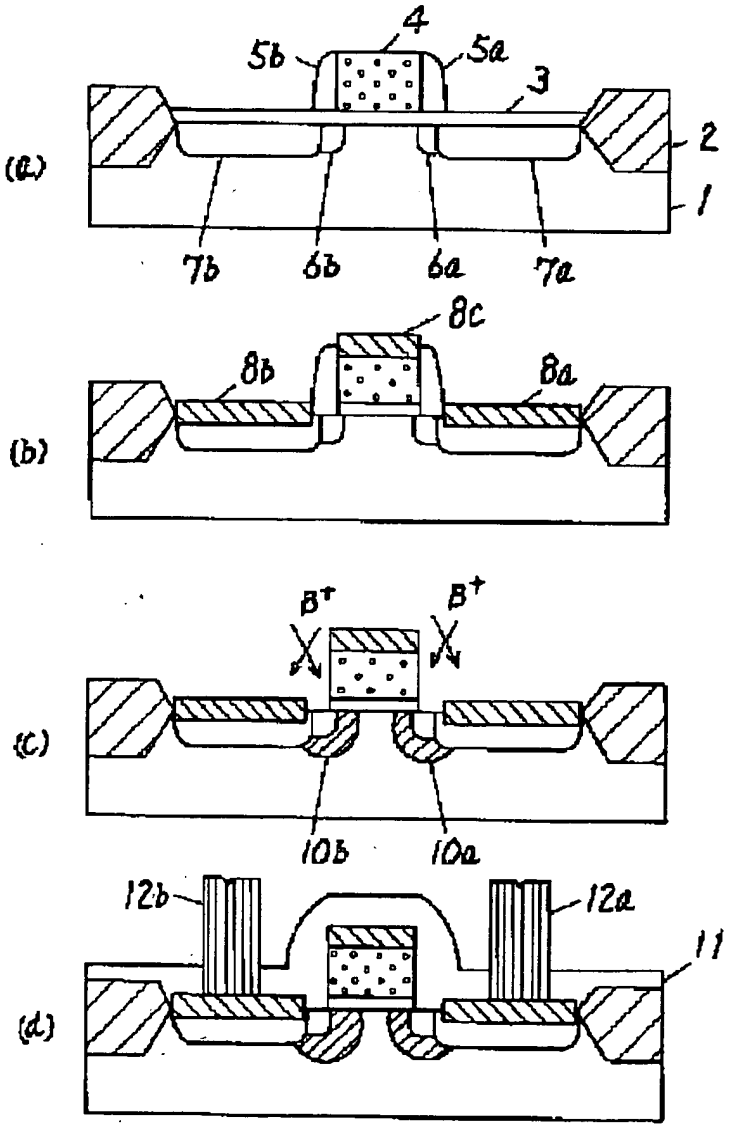
(74) Representative:

(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(57) Abstract:

PURPOSE: To provide the title semiconductor device and manufacturing method thereof capable of easily controlling the inversion voltage making high breakdown strength and high driving force compatible with each other without increasing the capacities of source and drain.

CONSTITUTION: After removing the residual insulating films 5a, 5b on the sidewalls of a gate electrode 4, P+ type semiconductor layers 10a, 10b are selectively implanted in the end parts only on the channel side of source-drain 6a, 6b. The P+ type semiconductor layers 10a, 10b can restrain the punch-through of source, drain to control the inversion voltage thereby enabling the concentration of a P type substrate to be set up at low level as well as an element to be microminiaturized without increasing the drain capacity at all. Furthermore, the impurity concentration in the channel region can be unequalized thereby increasing the driving force of transistors.



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国際事務局

特許協力条約に基づいて公開された国際出願

(51) 国際特許分類6 H01L 29/786	A1	(11) 国際公開番号	WO97/06564
		(43) 国際公開日	1997年2月20日(20.02.97)

(21) 国際出願番号 PCT/JP96/02184

(22) 国際出願日 1996年8月2日(02.08.96)

(30) 優先権データ

特願平7/200657	1995年8月7日(07.08.95)	JP
特願平7/210410	1995年8月18日(18.08.95)	JP
特願平7/210412	1995年8月18日(18.08.95)	JP

(71) 出願人（米国を除くすべての指定国について）
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(75) 発明者／出願人（米国についてのみ）
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池田隆英(IKEDA, Takahide)[JP/JP]
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山口 憲(YAMAGUCHI, Ken)[JP/JP]
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(74) 代理人
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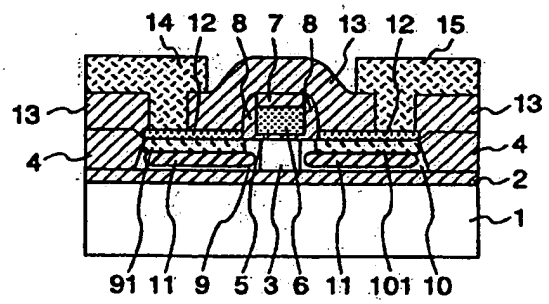
〒100 東京都千代田区大手町2丁目2番1号
新大手町ビル331 Tokyo, (JP)

(81) 指定国 CN, JP, KR, SG, US, 欧州特許 (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

添付公開書類
国際調査報告書

(54)Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

(54)発明の名称 半導体装置及びその製造方法



(57) Abstract

A parasitic bipolar where minority carriers (AS) produced in an SOI substrate (1) by injecting the carriers (AS) into the source of a MOS transistor formed on the substrate (1). An area having a conductivity which is opposite to that of the source diffused layer (11) of the MOS transistor and a recombination center mechanism is formed in the source diffused layer (11).

(19) (11) Publication number: 07050417 A

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PATENT ABSTRACTS OF JAPAN

(21) Application number: 05213548

(51) Intl. Cl.: H01L 29/786 H01L 21/20 H01L 21/84 H01L 27/12

(22) Application date: 06.08.93

(30) Priority:

(43) Date of application publication: 21.02.95

(84) Designated contracting states:

(71) Applicant: CANON INC

(72) Inventor: INOUE SHUNSUKE

(74) Representative:

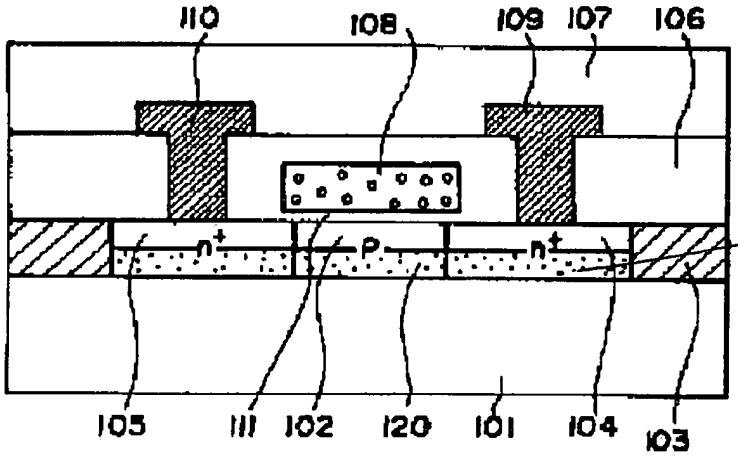
(54) SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: To make high mobility and low life time of a carrier compatible by a method wherein the carrier life time in the part in contact with a part of active region is to be arranged in the low life time region smaller than the active region.

CONSTITUTION: An active region on an insulating substrate 101 is composed of a p type channel region 102, an n+source region 105, an n+drain region 104, a gate insulating film 111, and a polysilicon gate 108. On the other hand, the surface side near the polysilicon gate 108 is provided with single crystal or quasi-crystal while a low life time region 120 e.g. polycrystalline or amorphous, etc., is provided on the part near the insulating substrate 101 side. Through these procedures, the low life time layer 120 can suppress the hole accumulation to immediately extingluish the hole in the low life time region 120 so that the deterioration in the breakdown strength due to the carrier accumulation as well as the fluctuation in inverse voltage in the channel region 102 may be suppressed.

(a)



(b)